veriT: System Description for SMT-COMP 2018

Haniel Barbosa[1], Daniel El Ouraoui[2], Pascal Fontaine[2], Hans-Jörg Schurr[2⋆]

[1] University of Iowa, Iowa City, USA
haniel-barbosa@uiowa.edu
[2] CNRS, Inria, and the University of Lorraine, Nancy, France;
{daniel.elouraoui, pascal.fontaine, hans-jorg.schurr}@loria.fr

URL : http://www.verit-solver.org — Seed : 55315

veriT is a satisfiability modulo theory (SMT) solver developed by University of Lorraine, Inria (Nancy, France). veriT provides an open, trustable and reasonably efficient decision procedure [3] for the logic of quantifier-free formulas over uninterpreted symbols, linear real arithmetics, and the combination thereof. It also handles linear arithmetics over integers, and has quantifier reasoning using trigger- and conflict-based instantiation [2] as well as enumerative instantiation [6]. Finally, veriT is proof-producing [5, 1]. veriT is written in C and accepts the input formats SMT-LIB 2.6 and DIMACS. It integrates a CDCL($\mathcal{T}$)-based Boolean satisfiability engine with a Nelson-Oppen like combination of decision and semi-decision procedures with propagation of model equalities, and implements simplifications such as symmetry-based reductions [4]. The tool is open-source and distributed under the BSD licence.

The veriT version competing in SMT-COMP 2018 is similar to the entry of 2017. It has seen general improvements to the infrastructure, but no changes that should affect the performance in the competition in major ways.

veriT participates in the following divisions: ALIA AUFLIA AUFLIRA LIA UF UFIDL UFLIA UFLRA QF_ALIA QF_AUFLIA QF_IDL QF_LIA QF_LRA QF_RDL QF_UF QF_UFIDL QF_UFLIA QF_UFLRA.

Acknowledgements The development of veriT is funded by the project H2020-FETOPEN-2016-2017-CSA SC^2 (712689) and by the European Research Council (ERC) starting grant Matryoshka (713999).

References

1. H. Barbosa, J. C. Blanchette, and P. Fontaine. Scalable fine-grained proofs for formula processing. In L. de Moura, editor, *Proc. Conference on Automated Deduction (CADE)*, Lecture Notes in Computer Science. Springer Berlin Heidelberg, 2017.
2. H. Barbosa, P. Fontaine, and A. Reynolds. Congruence closure with free variables. In A. Legay and T. Margaria, editors, *Tools and Algorithms for Construction and Analysis of Systems (TACAS)*, volume 10206 of *Lecture Notes in Computer Science*, pages 214–230, 2017.

⋆ The author order is strictly alphabetic.

3. T. Bouton, D. C. B. de Oliveira, D. Déharbe, and P. Fontaine. veriT: an open, trustable and efficient SMT-solver. In R. A. Schmidt, editor, *Proc. Conference on Automated Deduction (CADE-22)*, 2009.
4. D. Déharbe, P. Fontaine, S. Merz, and B. Wolzenlogel Paleo. Exploiting Symmetry in SMT Problems. In N. Bjørner and V. Sofronie-Stokkermans, editors, *Proc. Conference on Automated Deduction (CADE-23)*, 2011.
5. D. Déharbe, P. Fontaine, and B. Wolzenlogel Paleo. Quantifier Inference Rules for SMT proofs. In *First Workshop on Proof eXchange for Theorem Proving (PxTP)*, 2011.
6. A. Reynolds, H. Barbosa, and P. Fontaine. Revisiting enumerative instantiation. volume 10806 of *Lecture Notes in Computer Science*, pages 112–131. Springer, 2018.