veriT: System Description for SMT-COMP 2016

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veriT is a satisfiability modulo theory (SMT) solver jointly developed by University of Lorraine, Inria (Nancy, France) and Federal University of Rio Grande do Norte (Natal, Brazil). veriT provides an open, trustable and reasonably efficient decision procedure [1] for the logic of unquantified formulas over uninterpreted symbols, linear real arithmetics, and the combination thereof. It also handles linear arithmetics over integers, and has quantifier reasoning using trigger instantiation based on E-matching. Finally, veriT is proof-producing [3].

veriT is written in C and accepts the input formats SMT-LIB 2.0 and DIMACS. It integrates a DPLL-based Boolean satisfiability engine with a Nelson-Oppen like combination of decision and semi-decision procedures with propagation of model equalities, and implements simplifications such as symmetry-based reductions [2]. The tool is open-source and distributed under the BSD licence.

Since SMT-COMP 2015, veriT has seen various little improvements. Support for non-linear arithmetics is however still unstable. Support for quantifier reasoning has been greatly improved, and is still under development. Due to lack of time, the submitted version is experimental. A distribution, featuring all recent improvements and proof production will be released soon.

veriT participates in the following divisions: ALIA AUFLIA AUFLIRA LIA LRA QF_ALIA QF_AUFLIA QF_IDL QF_LIA QF_LRA QF_NRA QF_RDL QF_UF QF_UFIDL QF_UFLIA QF_UFLRA UF UFIDL UFLIA UFLRA.

References

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