SMT-COMP 2014 entry: CVC4 v1.4

CVC4 is a tool for determining the satisfiability of a first order formula modulo a first order theory (or a combination of such theories). It is the fourth in the Cooperating Validity Checker family of tools (CVC, CVC Lite, CVC3) but does not directly incorporate code from any previous version.

CVC4 is an open and extensible SMT engine. It can be used as a stand-alone tool or as a library. It has been designed to increase the performance and reduce the memory overhead of its predecessors, especially CVC3. It is written entirely in C++ and is released under an open-source license.

More information about CVC4 is available in [1] and at its website: http://cvc4.cs.nyu.edu/

Divisions in main track: all Divisions in application track: all

Expected Performance: CVC4 has been carefully engineered for performance. We are competing in all divisions as a testament to how broadly applicable CVC4 is. We don't expect to perform particularly well in difference logic (as we aren't using a specialized difference logic solver) or in logics with nonlinear arithmetic, where support is planned but currently lacking. We expect it to perform competitively in most logics.

New Functionality Of particular relevance to the competition are significant improvements made in three areas: quantifiers, arithmetic reasoning, and bit-vector reasoning. The improvements to quantifiers are based on finite-model finding and other advanced techniques, some of which are described in Andrew Reynolds' PhD thesis [4]. The improvements in arithmetic reasoning are from a new Sum-Of-Infeasibilities Simplex algorithm [3] as well as an integration with the GLPK solver (as-yet-unpublished work by Timothy King). The Bit-vector solver is a portfolio solver, running both a lazy and an eager solver, as described in [2].

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CVC4 incorporates code from MiniSAT for propositional reasoning.

Magic #: 44444

References

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- [2] Liana Hadarean, Clark Barrett, Dejan Jovanović, Cesare Tinelli, and Kshitij Bansal. A tale of two solvers: Eager and lazy approaches to bit-vectors. In *Proceedings of the* 26th International Conference on Computer Aided Verification (CAV '14), Lecture Notes in Computer Science. Springer, July 2014. Vienna, Austria, to appear.
- [3] Timothy King, Clark Barrett, and Bruno Dutertre. Simplex with sum of infeasibilities for SMT. In Proceedings of the 13th International Conference on Formal Methods In Computer-Aided Design (FMCAD '13), pages 189–196. FMCAD Inc., October 2013. Portland, Oregon.
- [4] Andrew Reynolds. Finite Model Finding in Satisfiability Modulo Theories. PhD thesis, University of Iowa, December 2013.