veriT+raSAT+Redlog: System Description for SMT-COMP 2017

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veriT+raSAT+Redlog is an SMT solver based on the SMT solver veriT [2] with a combination the following two solvers for solving nonlinear arithmetic.

1. raSAT loop [6, 5] which is an extension of Interval Constraint Propagation [1] with testing and the application of the Intermediate Value Theorem (IVT).
2. Redlog [3] is a key component of the open-source computer algebra system Reduce. It supplements Reduce's comprehensive collection of methods from symbolic computation with 100+ functions operating on formulas in interpreted first-order logic. Formulas co-exist and share data structures with conventional objects of symbolic computation within one homogeneous system. Within a rich infrastructure of methods on first-order formulas, Redlog has a strong focus on quantifier elimination and decision procedures for various algebraic theories.

The combination is similar to the idea from [4] where when each box of ICP becomes smaller than a threshold ϵ, a complete framework (CAD) is called to solve the remaining unknown constraints over such a small box. The main difference here is that when all boxes of raSAT loop become smaller than ϵ, Redlog is utilized to solve the unknown constraints with the box contracted from $[-\infty, \infty]^n$ where n is the number of variables. As a result, for a conjunction of polynomial constraints, Redlog is called only once from raSAT loop. While Redlog complements raSAT loop in the completeness, the small box of raSAT loop assists Redlog to prune its searching space. At this moment, ϵ is set to $\frac{0.125}{8}$ by default, which is experimentally selected based on the performances of different values of ϵ.

veriT+raSAT+Redlog participates in the following divisions: QF_NRA and QF_UFNRA.

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