veriT+Redlog: System Description for SMT-COMP 2017

Haniel Barbosa[1], Pascal Fontaine[1], Maximilian Jaroschek[5], Marek Kosta[4], Thomas Sturm[1,3], Vu Xuan Tung[2⋆]

[1] University of Lorraine, CNRS, Inria, and LORIA, Nancy, France;
{haniel.barbosa,thomas.sturm,pascal.fontaine}@loria.fr
[2] Japan Advanced Institute of Science and Technology
tungvx@jaist.ac.jp
[3] MPI Informatics and Saarland University, Saarbrücken, Germany;
sturm@mpi-inf.mpg.de
[4] Slovak Academy of Sciences, Bratislava, Slovak Republic;
marek.kosta@savba.sk
[5] Technische Universität Wien, Vienna, Austria
mjarosch@forsyte.at

URL : http://www.verit-solver.org — Seed : 20170605

veriT is a satisfiability modulo theory (SMT) solver jointly developed by University of Lorraine, Inria (Nancy, France) and Federal University of Rio Grande do Norte (Natal, Brazil). veriT provides an open, trustable and reasonably efficient decision procedure [3] for the logic of quantifier-free formulas over uninterpreted symbols, linear real arithmetics, and the combination thereof. It also handles linear arithmetics over integers, and has quantifier reasoning using trigger- and conflict-based instantiation [2]. Finally, veriT is proof-producing [5, 1]. veriT is written in C and accepts the input formats SMT-LIB 2.6 and DIMACS. It integrates a CDCL($\mathcal{T}$)-based Boolean satisfiability engine with a Nelson-Oppen like combination of decision and semi-decision procedures with propagation of model equalities, and implements simplifications such as symmetry-based reductions [4]. The tool is open-source and distributed under the BSD licence.

Redlog [6] is a key component of the open-source computer algebra system Reduce. It supplements Reduce's comprehensive collection of methods from symbolic computation with 100+ functions operating on formulas in interpreted first-order logic. Formulas co-exist and share data structures with conventional objects of symbolic computation within one homogeneous system. Within a rich infrastructure of methods on first-order formulas, Redlog has a strong focus on quantifier elimination and decision procedures for various algebraic theories.

This submission implements a CDCL($\mathcal{T}$) loop that uses Redlog as an "instantiation module": since the supported logics admit quantifier elimination, quantifier-free equivalent instances are generated by Redlog for the asserted quantified formulas and veriT then proceeds with the given instances.

veriT+Redlog participates in the following divisions: LRA NRA.

⋆ The author order is strictly alphabetic.

Acknowledgements The development of veriT and the development of the SMT features of Redlog are funded by the projects ANR-13-IS02-0001-01 & DFG STU 483/2-1 SMArT and H2020-FETOPEN-2016-2017-CSA SC^2 (712689)

References

1. H. Barbosa, J. C. Blanchette, and P. Fontaine. Scalable fine-grained proofs for formula processing. In L. de Moura, editor, *Proc. Conference on Automated Deduction (CADE)*, Lecture Notes in Computer Science. Springer Berlin Heidelberg, 2017.
2. H. Barbosa, P. Fontaine, and A. Reynolds. Congruence closure with free variables. In A. Legay and T. Margaria, editors, *Tools and Algorithms for Construction and Analysis of Systems (TACAS)*, volume 10206 of *Lecture Notes in Computer Science*, pages 214–230, 2017.
3. T. Bouton, D. C. B. de Oliveira, D. Déharbe, and P. Fontaine. veriT: an open, trustable and efficient SMT-solver. In R. A. Schmidt, editor, *Proc. Conference on Automated Deduction (CADE-22)*, 2009.
4. D. Déharbe, P. Fontaine, S. Merz, and B. Wolzenlogel Paleo. Exploiting Symmetry in SMT Problems. In N. Bjørner and V. Sofronie-Stokkermans, editors, *Proc. Conference on Automated Deduction (CADE-23)*, 2011.
5. D. Déharbe, P. Fontaine, and B. Wolzenlogel Paleo. Quantifier Inference Rules for SMT proofs. In *First Workshop on Proof eXchange for Theorem Proving (PxTP)*, 2011.
6. A. Dolzmann and T. Sturm. Redlog: Computer algebra meets computer logic. *ACM SIGSAM Bulletin*, 31(2):2–9, 1997.