veriT: System Description for SMT-COMP 2014

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URL : http://www.verit-solver.org — Seed : 1027

veriT is a satisfiability modulo theory (SMT) solver jointly developed by University of Lorraine, Inria (Nancy, France) and Federal University of Rio Grande do Norte (Natal, Brazil). veriT provides an open, trustable and reasonably efficient decision procedure [1] for the logic of unquantified formulas over uninterpreted symbols, linear real arithmetics, and the combination thereof. It also handles linear arithmetics over integers, as well as quantifier reasoning capabilities through E-matching. Finally, veriT includes proof-production capabilities [3].

veriT is written in C and accepts the following input formats: SMT-LIB 2.0 and DIMACS. It integrates a DPLL-based Boolean satisfiability engine with a Nelson-Oppen like combination of decision and semi-decision procedures with propagation of model equalities, and implements simplifications such as symmetry-based reductions [2]. The tool is open-source and distributed under the BSD licence.

Since its last participation at SMT-COMP, veriT has been completely rewritten and features an improved decision procedure for linear real arithmetics. Ongoing developments include improving combination inside the solver, support for non-linear arithmetics, integers and quantifier reasoning.

veriT participates in the 2014 edition of SMT-COMP in the following divisions: QF_UF, QF_RDL, QF_LRA, QF_UFLRA, QF_IDL, QF_LIA, QF_UFLIA, AUFLIA, AUFLIRA.

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References

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